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Harmonic Performance Evaluation of SPWM-Controlled Seven-Level Single-Phase Diode-Clamped Multilevel Inverters across Variable Modulation Indices

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Abstract

Multilevel inverters (MLIs) are crucial in medium-voltage high-power applications due to their high-power quality and reduced electromagnetic interference. Among different topologies, the diode-clamped MLI (DCMLI) offers a robust structure. This paper presents a harmonic performance evaluation of SPWM-controlled seven-level single-phase DCMLI across variable modulation indices. The performance evaluation techniques include Phase Disposition (PD), Alternative Phase Opposition Disposition (APOD), and Phase Opposition Disposition (POD). A rigorous simulation model is developed in MATLAB/Simulink to evaluate the output voltage THD across a wide range of modulation indices (Ma) of 0.4 to 1.2 in steps of 0.1 and an M_a = 1.0 using PD strategy (THD=8.5%). The results demonstrate that the PD strategy consistently yields the lowest THD of (8.5%) across the linear modulation range (Ma < 1.0), while the performance in the over modulation region varies distinctly between strategies. This study provides a clear guideline for selecting the optimal SPWM strategy for a seven-level diode-clamped multi-level inverter based on the desired operating modulation index to minimize harmonic content and enhance power quality.

Keywords – Alternate phase opposition disposition (APOD), Phase disposition (PD), Phase opposition disposition (POD), Pulse width modulation (PWM), Total harmonic distortion (THD) Multilevel Inverter, Diode-Clamped Inverter, Modulation Index Power Quality, Harmonic Analysis.

1. Introduction

The process through which the Inverter converts DC power supply to AC power supply is called inversion. This inversion process is the reverse of the rectifier process, where the AC supply is converted into DC power supply (Amah and Mom, 2019).

The input voltage, output voltage and frequency of an inverter depend on the design of the circuit. A power inverter can be entirely electronics or may be a combination of mechanical effects and electronic circuit (Amah and Mom, 2019).

The global shift towards renewable energy integration and advanced motor drives has necessitated the development of efficient and high-fidelity power conversion systems. The conventional two-level inverters suffer from high dv/dt stress, significant electromagnetic interference (EMI), and substantial harmonic distortion, especially at lower switching frequencies (Kashappa, 2024). Multilevel Inverters (MLIs) have emerged as a superior alternative, synthesizing a stepped output voltage waveform that closely matehes a sinewave, thereby inherently reducing harmonic content (Mahato, et al., 2022). The diode-clamped MLI (DCMLI), introduced by Nabae et al. (1981), is a fundamental topology that utilizes clamping diodes to create multiple voltage levels across the DC bus. A seven-level inverter, for instance, can generate output voltages with significantly lower Total Harmonic Distortion (THD) when compared to the three- or five-level counterparts (Kashappa, 2024), making it proper for grid-connected photovoltaic systems and medium-voltage industrial applications (Ansari and Gupta 2021). Performances of MLIs are influenced by their modulation strategies. Among the techniques of carrier-based Sinusoidal Pulse Width Modulation (SPWM) is widely adopted because of its simplicity and effectiveness (Amah, and Mom, 2019) (McGrath, and Holmes 2002). However, the phase relationship between the multiple carrier signals can be arranged in different dispositions Phase (PD), Phase Opposition (POD), and Alternative Phase Opposition (APOD) with each of them generating unique switching patterns and, consequently, different harmonic spectra (Amah and Mom 2019). While existing literature has explored SPWM strategies for three-level and five-level inverters, a comprehensive and comparative study focusing on a seven-level diode-clamped inverter over a wide range of modulation indices (including the over modulation region) is lacking. The gap is critical because the harmonic performance in the over modulation region is non-linear and strategy-dependent. This paper presents a systemic harmonic performance evaluation of SPWM-controlled 7L- single-phase DCMLI across variable modulation indices using PD, POD, and APOD SPWM strategies. The analysis is conducted for modulation indices from 0.4 to 1.2, by providing crucial insights for engineers to select the optimal modulation technique based on their specific operational requirements for minimal harmonic distortion

1.1 Literature Review

The MLIs foundation was established with the three-level neutral-point clamped inverters (Vodovozov, 2010). Later, other researches have expanded into numerous topologies like flying capacitor and cascaded H-bridge, each with distinct advantages (Gonshwe, et al., 2016). The popularity of DCMLI was based on its structural simplicity and ease of extension to higher levels, though it faces challenges in capacitor voltage balancing at higher levels and for a seven-level DCMLI, THD values which typically decreases as the modulation index approaches unity. For instance, in a one study reports that THD is minimized at higher modulation indices, and further reduction is possible with the addition of an LC filter (Rusdi, et al., 2021).

The role of critical modulation strategies in determining MLI performance was well-documented with the SPWM techniques using multiple carriers were first generalized in the studies of McGrath and Holmes (2002). Reddy, (2020), provided a well detailed spectral analysis for different multicarrier PWM techniques, establishing the PD-PWM which generally offers a better harmonic performance for linear modulation in a three-phase system. Lokeshwar, et al. (2017) opined in their work of the seven-level diode clamed inverters where the basic fundamental components of output voltage an a THD using the SPWM, THIPM and SVPWM strategic modulation.

Yuditya, et al. (2020) compared the in a performance of MLI of single-phase with sinusodal pulse width modulation of unipolar and bipolar techniques for switiching considered the level of increment in single phase MLI that effectively reduces the harmonic distortion and SPWM of the unipolar switchning signal which produces a lower value for THD than the bipolar technique. The work in (Shaji, et al., 2020) the new 7-level switched capacitor multilevel inverter topology with low voltage rating switches and single voltage source shows promising performance and low THD when driven using various PWM techniques. In the analyses the works did not consider DCMLI but did not venture into the seven-level domain or provide a detailed map of THD versus modulation index for all major SPWM dispositions. This paper aims to fill this specific void by providing a granular, strategy-wise THD analysis for a 7L-DCMLI

2. Design and Analysis

2.1 System Block Diagram

Figure. 1 shows the block diagram of a single phase seven level Diode Clamp multi-level inverter. The battery bank array generates the required DC voltage of 220Vdc that the boost converter (Mom, et al., 2019) steps up to 630Vdc which is controlled by PI controller for error handling. The step-up voltage is fed into a single phase seven level Diode Clamp MLI using optimized SPWM to generate switching pulses for the inverter switches which produce a seven-level output voltage of 220Vac for household load consumption (Amah and Mom 2019).

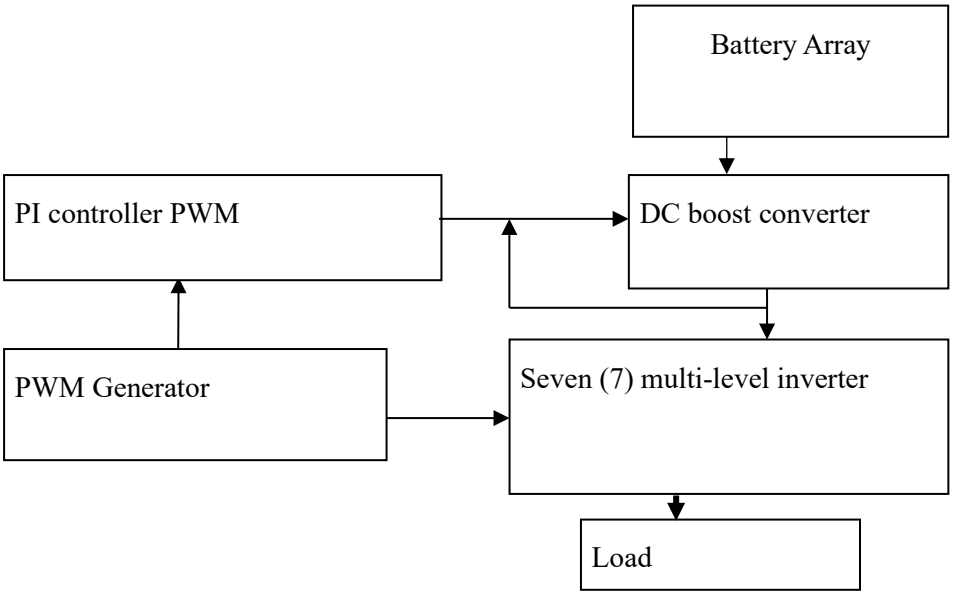

Figure 1: The block diagram of seven-level the single-phase Diode-Clamp inverter.

2.2 Circuit Configuration and Operational Principle Seven-Level Diode-Clamped Inverter Topology

The seven-level single-phase DCMLI circuit requires 12 switching devices (S1-S12), 10 clamping diodes, and a DC bus split into six capacitors (C1-C6) (6) (n-1) where n=7 to create three intermediate voltage levels (Vdc/6, Vdc/3, Vdc/2, 2Vdc/3, 5Vdc/6) in addition to 0 and Vdc. The capacitors are assumed to be pre-balanced and large enough to maintain stable voltages. The output voltage (V_out) is taken between the inverter mid-point and the neutral point of the capacitor bank.

The circuit in Figure. 2 shows a seven-level single phase DCMLI, this DCMLI consists of six switching pairs (S1, S7), (S2, S8), (S3, S9), (S4, S10), (S5, S11) and (S6, S12). If one switch of the pair is switched on, the other complementary switch of same pair must be off. The DC-link capacitors together with the diodes clamp the switching voltage to half level of the DC bus voltage while the neutral (N) is the reference point of the circuit. To obtain switching combination so as to obtain the required output voltage level for a seven-level DCMLI is as shown in Table 1.

The structural arrangement of the seven-level single phase DCMLI is powered by a single DC source with an appropriate switching of the semi-conductor switches in the modules. Each of the phases produces seven output voltage levels. The switching patterns for the different voltage levels are as presented in Table 1.

A single sinusoidal reference wave (V_ref) of frequency 50 Hz and amplitude modulated by the modulation index (M_a) is compared with six triangular carrier waves (V_carr) of frequency 2 kHz (f_carr). The carrier waves are arranged in three disposition (Amah and Mom 2019):

Phase Disposition (PD): All six carrier waves are in phase with each other.

Phase Opposition Disposition (POD): The carrier waves above the zero reference are in phase with each other but 180° out of phase with those below the zero reference.

Alternative Phase Opposition Disposition (APOD): Every adjacent carrier wave is phase-shifted by 180°.

The modulation index is defined as $Ma = \frac{A\_m}{(M*A\_c)}$,

where A_m is the amplitude of the reference signal, A_c is the amplitude of each carrier signal, and m is the number of carrier signals (m=6). M_a is varied from 0.4 to 1.2 in steps of 0.1.

2.3. Simulation Setup

The system is modelled and simulated in MATLAB/Simulink R2023a using the Simscape Electrical™ library. The DC link voltage (V_dc) is set to 600V. The switching devices are ideal IGBTs with anti-parallel diodes. A fast Fourier transform (FFT) analysis tool is used to analyze the output voltage waveform and calculate the THD over 40 cycles (to ensure steady-state) for each simulation run. The THD is calculated up to the 50th harmonic.

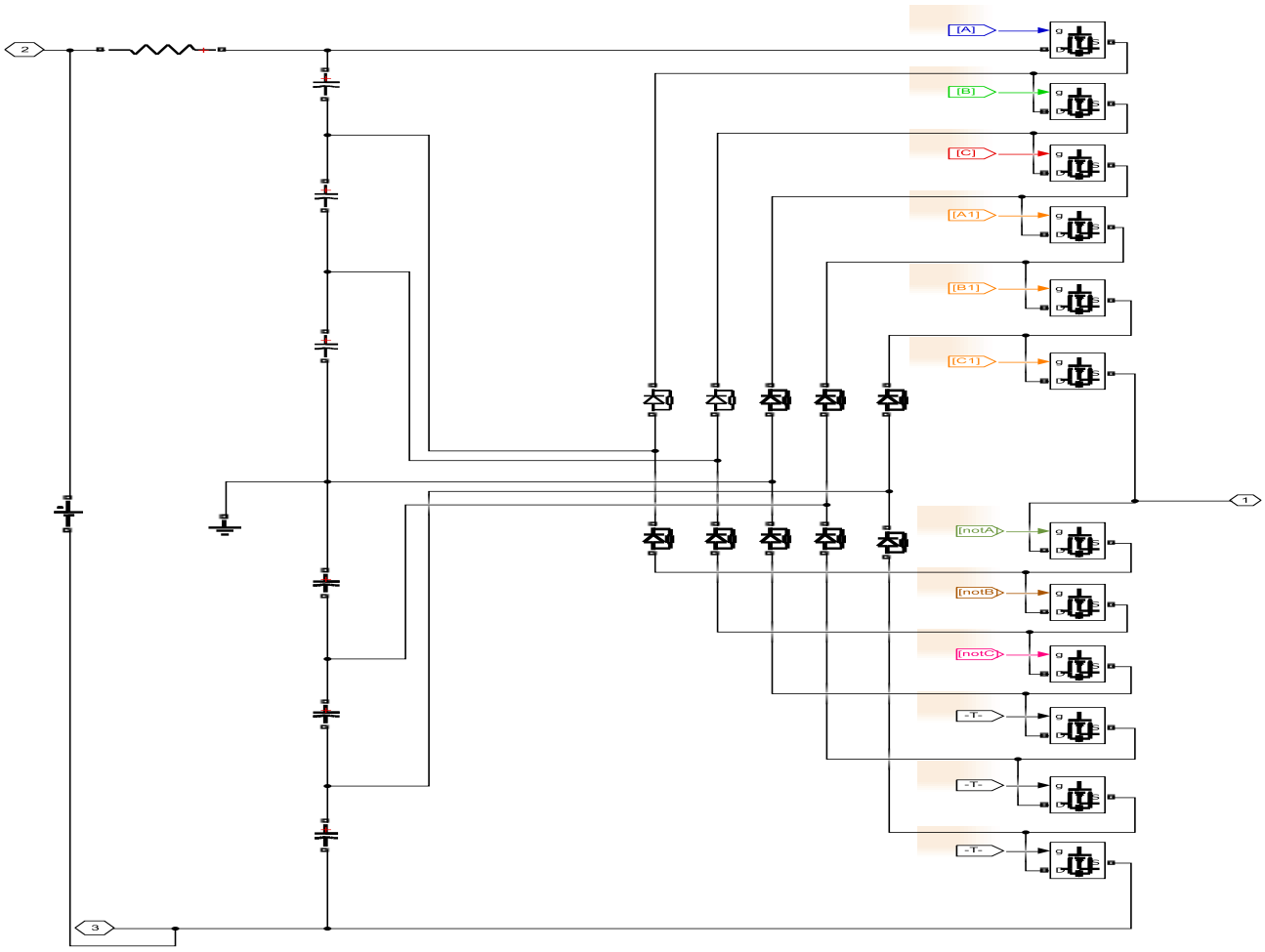

Figure 2: Seven-Level Single-phase Diode Clamped Multi-Level Inverter.

Table 1: Switching states of a Seven-level DC MLI

Output Voltage Level	Switching States											
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
Vdc/2	1	1	1	1	1	1	0	0	0	0	0	0
Vdc/3	0	1	1	1	1	1	1	0	0	0	0	0

Vdc/6	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	0
-Vdc/6	0	0	0	0	1	1	1	1	1	1	0	0
-Vdc/3	0	0	0	0	0	1	1	1	1	1	1	0
-Vdc/2	0	0	0	0	0	0	1	1	1	1	1	1

3. Design of Inverter Control Circuit

The Modeling of Switching Logic Equations

Traditionally the operation of a seven-level single-phase diode clamped inverter requires six carrier (n-1=7-1=6) signals and a single modulating waveform. These signals combine to produce pulses for the switching of the twelve inverter switches. The analysis of the combination of the signals is as follows (Reddy, 2020). G is the modulating signal m(t), A is the pulse obtained when the modulating signal m(t) and the carrier signal $r\__1$ (t) with [10 12] output values are compared, $A\__1$ is the pulse produced when m(t) and $r\__2$ (t) with [8 10] output values are compared, $A\__2$ is the resulting pulse when m(t) and $r\__3$ (t) with output values [6 8] are compared, B pulse results when m(t) and $r\__4$ (t) with [4 6] output values are compared, when m(t) and $r\__5$ (t) [2 4] are compared $B\__1$ pulse is produced ,$B\__2$ is the pulse obtained by comparing m(t) and $r\__6$ (t) with [0 2] values. The combination of these pulses triggers the switches numbered from $S\__1$ to $S\__{12}$.

The equations developed from the analysis of the signals are given by equations (24) to (35). (Gonshwe et al., 2016)

$S_1 = A.\bar{G} + \bar{A}.G$ (24)
$S_4 = A.G + \bar{A}.\bar{G}$ (25)
$S_5 = A_1.\bar{G} + \bar{A}_1.G$ (26)
$S_8 = A_1.G + \bar{A}_1.\bar{G}$ (27)
$S_9 = A_2.\bar{G} + A_2.G$ (28)
$S_{12} = A_2.G + \bar{A}_2.\bar{G}$ (29)
$S_3 = B.\bar{G} + \bar{B}.G$ (30)
$S_2 = B.G + \bar{B}.\bar{G}$ (31)
$S_7 = B_1.\bar{G} + \bar{B}_1.G$ (32)
$S_6 = B_1.G + \bar{B}_1.\bar{G}$ (33)
$S_{11} = B_2.\bar{G} + B_2.G$ (34)
$S_{10} = B_2.G + \bar{B}_2.\bar{G}$ (35)

The modulation circuit for the single-phase of the inverter is designed using De Morgan's laws as shown in equations (36) to (47).

$S_1 = A \oplus G$ (36)
$S_4 = \overline{A \oplus G}$ (37)
$S_5 = A_1 \oplus G$ (38)
$S_8 = \overline{A_1 \oplus G}$ (39)
$S_9 = A_2 \oplus G$ (40)
$S_{12} = \overline{A_2 \oplus G}$ (41)
$S_3 = B \oplus G$ (42)
$S_2 = \overline{B \oplus G}$ (43)
$S_7 = B_1 \oplus G$ (44)
$S_6 = \overline{B_1 \oplus G}$ (45)
$S_{11} = B_2 \oplus G$ (46)
$S_{10} = \overline{B_2 \oplus G}$ (47)

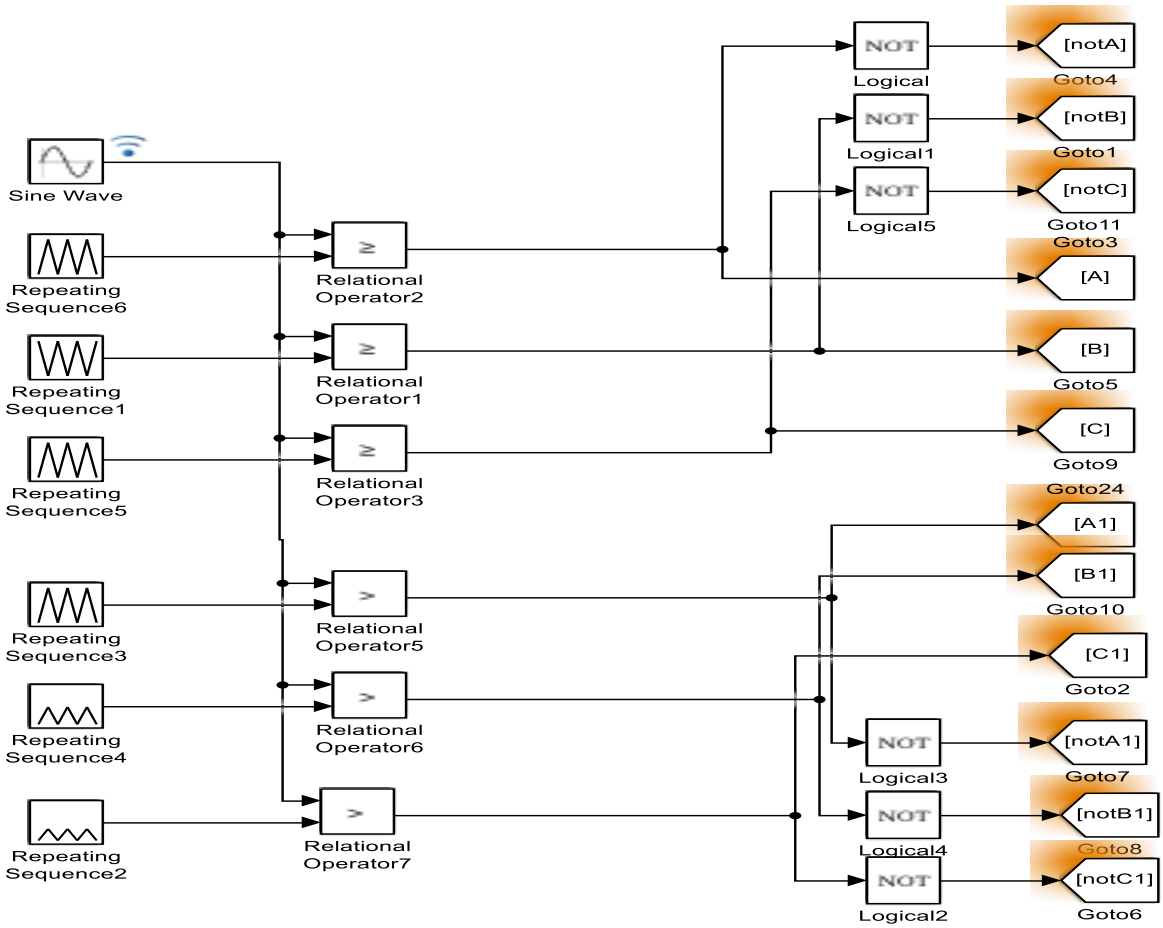

Figure 3: Sinusoidal reference and triangular carrier waves of PD SPWM for gating pulses

4. THD simulation of the Seven Level Single-Phase DCMLI for PD, POD and APOD at M.I = 0.4 to 1.2 using MATLAB/SIMULINK

The THD for the DCMLI was simulated for PD, POD and APOD SPWM techniques at varying modulation indexes of 0.4 to 1.2. The waveforms are as presented in Figure 4 to Figure 7.

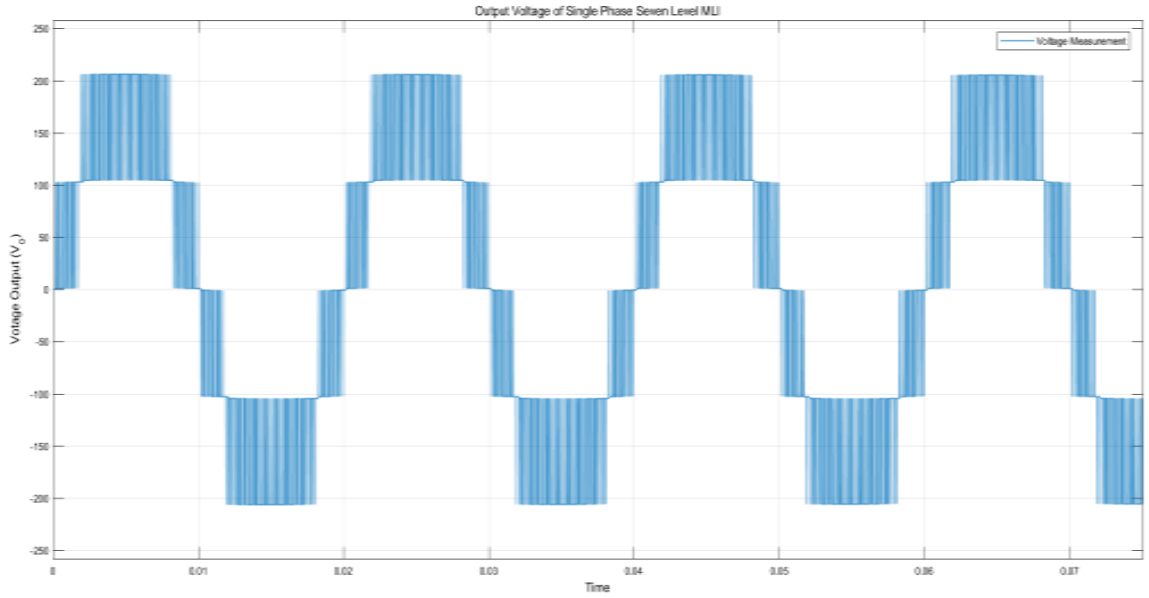

Figure 4: Voltage Output of a Seven-Level Single-Phase DCMLI on no load at m=0.1 to 0.7 for POD PWM

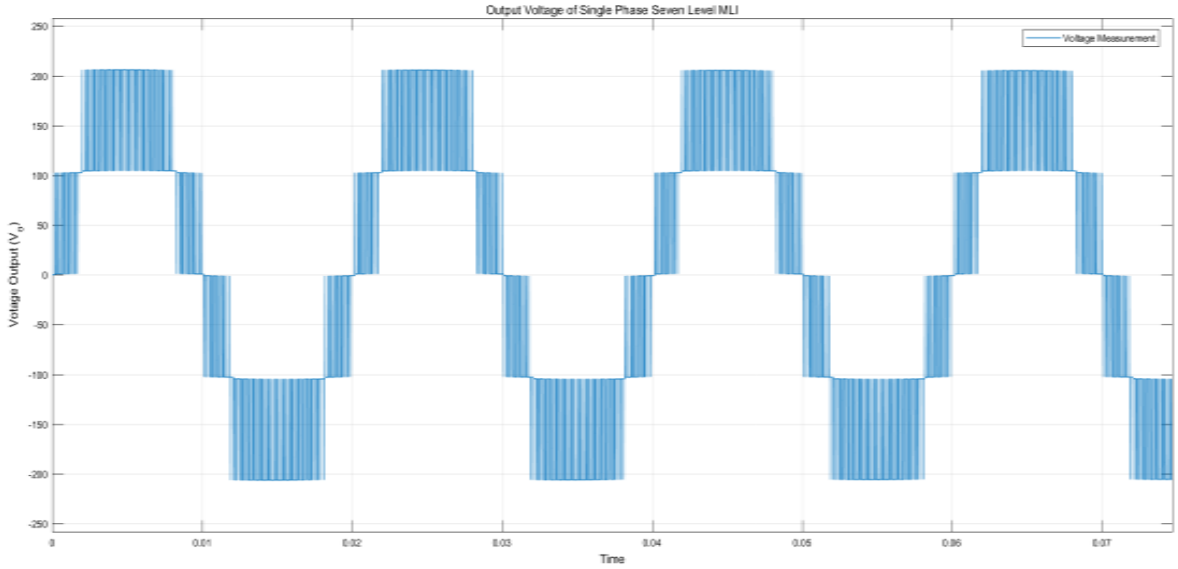

Figure 5: Voltage Output of a Seven-Level Single-Phase DCMLI on no load at m=0.6 for PD PWM

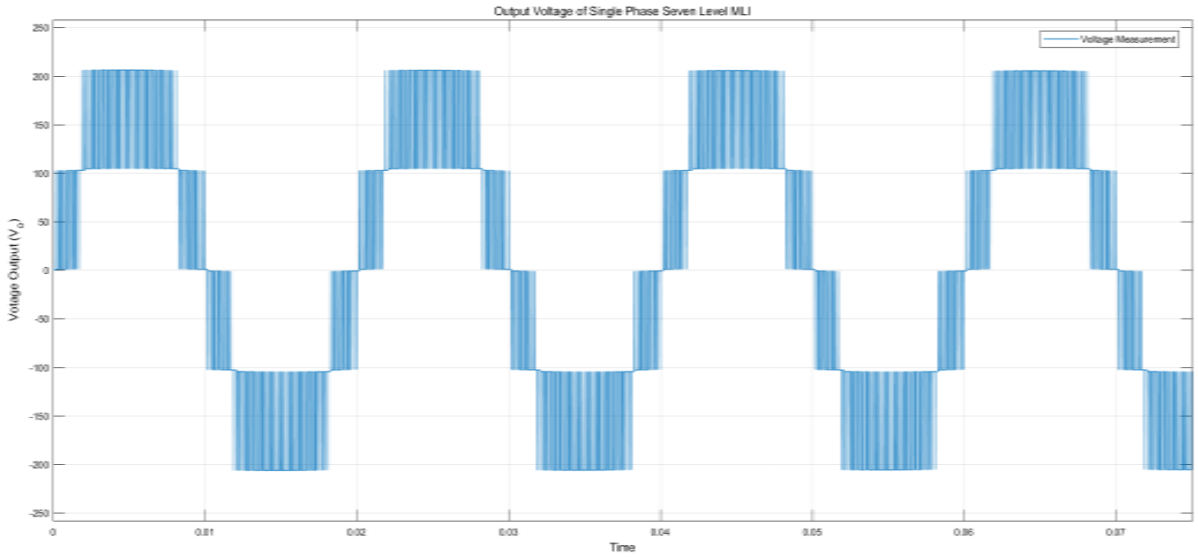

Figure 6: Voltage Output of a Seven-Level Single-Phase DCMLI on no load at m=0.6 for POD PWM

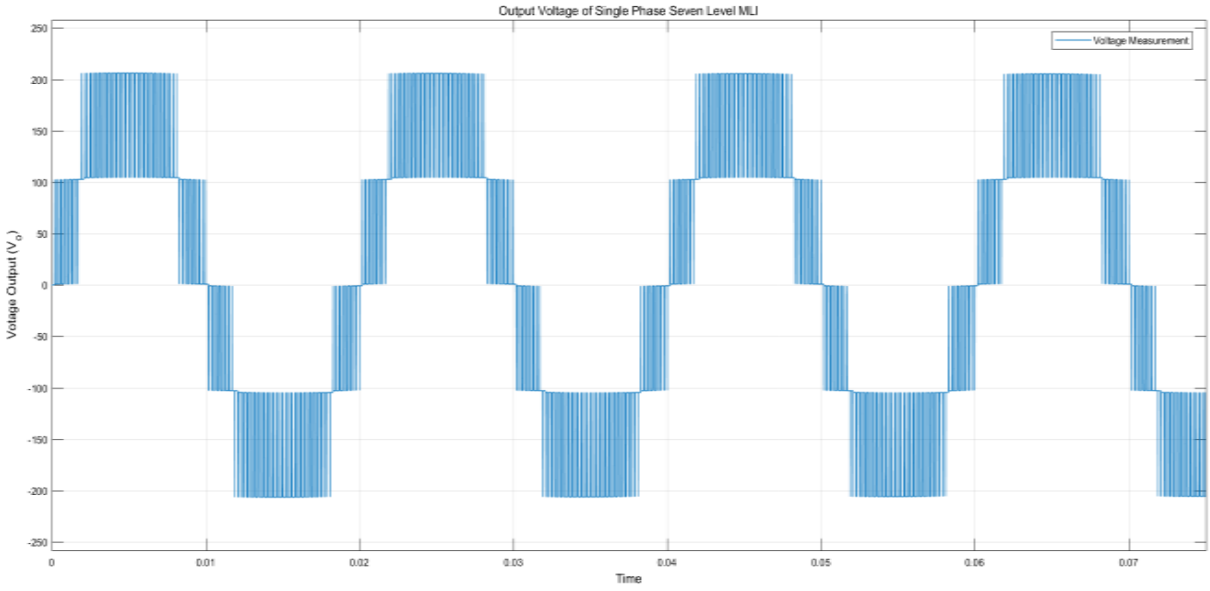

Figure 7: Voltage Output of a Single Phase Seven-Level DCMLI on no load at m=0.6 for APOD PWM

4.1 THD simulation of the seven-level single phase DCMLI for PD, POD and APOD at M.I = 0.4 to 1.2 using MATLAB/SIMULINK

The results analysis from frequency of PD, POD and APOD are summarized in Table 2 to Table 4.

Table 2: THD and Fundamental Magnitude of PD PWM Technique of Seven-level DC MLI

Modulation Index (M.I)	Fundamental Mag (50Hz)	Total Harmonic Distortion (THD) %
1.2	311.2	10.8
1.0	280.2	8.5
0.8	249.1	10.1
0.6	217.4	18.2
0.4	186.1	32.88

Table 3: THD and Fundamental Magnitude of POD PWM Technique of Seven-level DC MLI

Modulation Index (M.I)	Fundamental Mag. (50 Hz)	Total Harmonic Distortion (THD) %
1.2	311.2	9.9
1.0	280.2	11.09
0.8	249.1	13.5
0.6	217.4	22.1
0.4	186.1	34.4

Table 4: THD and Fundamental Magnitude of APOD PWM Technique of Seven-level DC MLI

Modulation Index (M.I)	Fundamental Mag. (50Hz)	Total Harmonic Distortion (THD) %
1.2	311.2	12.8
1.0	280.2	14.1
0.8	249.1	16.9
0.6	217.4	25.5
0.4	186.1	35.8

5. Discussion

From Table 2 to Table 4, it shows that the modulation index of 1.0 has the lowest THD values of 8.5 %, 11.2 % and 14.0 % respectively with fundamental frequency amplitudes of 280.2 for PD, POD and APOD SPWM in the FFT analysis of the seven-level single phase DCMLI. From Table 2, it shows that PD SPWM techniques has a better THD performance than PD and POD in a seven-level single-phase DCMLI due to low THD percentage recorded as 8.5 % with a magnitude of 280.2 over 3 cycles at a fundamental frequency of 50Hz over a maximum frequency of 1kHz. The results unequivocally demonstrate that the Phase Disposition (PD) strategy yields the superior harmonic performance for a 7L-DCMLI throughout the linear modulation range ($M_a \leq 1.0$). This is attributed to the constructive alignment of all carrier signals, which results in the effective switching frequency being multiplied by the number of carriers, pushing the dominant harmonic clusters to higher frequencies and making them easier to filter (Mahato, et al., 2022). The Alternative Phase Opposition Disposition (APOD) strategy consistently produced the highest THD. The alternating phase shifts between carriers create a more dispersed harmonic spectrum with a significant lower-order harmonics, which leads to a bad performance. The innovative finding is that the behavior in the over modulation region ($M_a > 1.0$). While the PD's THD starts increasing due to the losses of linearity and the disappearance of specific voltage levels, the strategy of POD shows a notable improvement. At $M_a=1.2$, POD's THD (9.5%) was lower than that of PD (10.8%). This crossover point is critical for applications requiring operation to be beyond the nominal voltage range. This

outcome phenomenon is because the POD disposition handles the saturation of the reference signal differently which leads to a more favorable harmonic cancellation in the over modulation region.

6. Conclusion

In this work, a design and development of a Seven-level Single-phase Diode Clamped MLI using PD SPWM technique has been achieved. The output of the inverter was observed to be 221.9V RMS with a THD of 8.5 % without filtering on no load which can be used at homes and the choice of optimal SPWM strategy is highly dependent on the operational modulation index.

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